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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,286	02/12/2002	Nicholas P. Wilt	210726	4895

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EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	3

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/074,286	Applicant(s) WILT ET AL.	
	Examiner Ulka J. Chauhan	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,13,14,16-26,28,29,34,35 and 37-42* is/are rejected.

7)☒ Claim(s) *5,9-12,15,27,30-33 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/9/02, 3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 6-8, 13, 14, 16-26, 28, 29, 34, 35, and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,844,569 to Eisler et al and U.S. Patent No. 6,753,878 to Heirich et al.

4. As per claim 1, Eisler teaches a computer system comprising:

a presentation surface set associated with the display device (c. 10 ll. 15-19: *A primary surface represents the pixmap image that the user is currently viewing on the display screen...the surface that the display hardware is currently reading and displaying on the monitor*);

a first display memory surface set associated with the first display source (c. 12 ll. 59-67 and Fig. 6: *video source 194 writes to the back buffer 196 associated with surface memory 204*) ;

a second display memory surface set associated with the second display source (c. 12 ll. 62-c. 13 ll. 10 and Fig. 6: *3D rendering system renders a graphical scene to the back buffer 206 associated with surface memory 206*; c. 8 ll. 56-64: *The display device interface 50 enables applications to access video memory including both off screen and on screen memory*; c. 11 ll. 14-16: *the application requests the interface to create a surface structure comprised of at least two surfaces, including a front and back buffer*; *therefore, plural applications creating surface structures are interpreted to be plural display sources having associated memory surfaces*); Eisler does not expressly teach:

a graphics arbiter, distinct from the first display source and from the second display source, for transferring display information from the first display memory surface set and from the second display memory surface set to the presentation surface set.

Heirich discloses an image generator 12 comprising a plurality of rendering engines 22, including double buffered frame buffers, a plurality of merge engines 24 and a frame store 26 (c. 5 ll. 31-33, c. 6 ll. 36-37, c. 12 ll. 44-47, and Fig. 1). Heirich discloses that one of the merge engines 24 is designated as the output merge engine which is provided with a data path to a frame buffer 26 and holds the output of image generator 12, which is a merged image of all of the part images PI (c. 6 ll. 31-35 and Fig. 1). And Heirich discloses that at each node, rendering can start as soon as both the previous rendering and the previous merging are finished (c. 21 ll. 63-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Eisler and Heirich whereby the merge engine structure/functionality taught by Heirich is implemented within Eisler's computer system so that

the flipping structures and presentation structure are decoupled to allow rendering and display to proceed in parallel and at different rates.

5. As per claim 2, Eisler discloses wherein the presentation surface set comprises a primary presentation surface and wherein the graphics arbiter transfers display information to the primary presentation surface (c. 13 ll. 1-10 and Fig. 6: *primary flipping structure comprises back buffer surface memory and primary surface memory*; c. 10 ll. 15-19: *A primary surface represents the pixmap image that the user is currently viewing on the display screen...the surface that the display hardware is currently reading and displaying on the monitor*).

6. As per claim 3, Eisler discloses wherein the presentation surface set comprises a presentation flipping chain, the presentation flipping chain comprising a primary presentation surface and a presentation back buffer, and wherein the graphics arbiter transfers display information to the presentation back buffer (c. 13 ll. 1-10 and Fig. 6: *primary flipping structure comprises back buffer surface memory and primary surface memory*; c. 10 ll. 15-19: *A primary surface represents the pixmap image that the user is currently viewing on the display screen...the surface that the display hardware is currently reading and displaying on the monitor*).

7. As per claim 4, Eisler disclose wherein transferring comprises transferring display information to portions of the presentation back buffer that are changed relative to a buffer immediately preceding the presentation back buffer in the presentation flipping chain (c. 13 ll. 1-10: *the 3D rendering system 198 renders a graphical scene to the back buffer 206 of the primary flipping structure 192. While the 3D rendering system renders the next frame to be displayed in the back buffer 204, the display controller 208 scans the current frame in the front buffer (primary surface) 210 to the display monitor 210*).

8. As per claim 6, Eisler discloses wherein the first display memory surface set comprises a display flipping chain (Fig. 6: *flipping structure 190*; c. 19 ll. 2-6: *If a BackBufferCount of "2" had been specified, two back buffers would have been created, and each call to the flip function would have rotated the surfaces in a circular pattern, providing a triple buffered flipping environment*).

9. As per claim 7, Heirich discloses that the merge unit includes components in the set: software executable, hardware, and firmware executable (Fig. 2).

10. As per claim 8, Eisler discloses that the flip function of the display device interface sets a register in the display hardware so that the exchange of the surface memory occurs when the display hardware performs a vertical retrace (c. 20 ll. 5-17). Eisler does not expressly teach wherein the graphics arbiter notifies. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented this functionality in combination with the merge engine structure/functionality in order to easily notify a safe flip condition.

11. As per claim 13, Eisler discloses that another optimization in the flip control is to read the scan line register to analyze the scan line position relative to the position when the last flip occurred (c. 24 ll. 43-45). Eisler does not expressly teach wherein the graphics arbiter notifies the first display source of a time when a scan line was displayed on the display device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented this functionality and horizontal sync signal in combination with the merge engine structure/functionality in order to easily notify a safe flip condition.

12. As per claim 14, Heirich discloses wherein the graphics arbiter enables processing by the first display source (c. 11 ll. 52-60: *Another operation is data broadcast, as might be used in*

connection with a multi-pass algorithm to render transparent surfaces, it will be necessary to broadcast data from one frame buffer to some or all other frame buffers. For example, a model containing transparent components can be rendered by first rendering all of the opaque components, merging the results, and then reloading all of the Z buffers with the merged Z result before proceeding to render the transparent components).

13. As per claim 16, Heirich discloses wherein the graphics arbiter transforms display information from the first display memory surface set (Fig. 2: *decoder 126,core 110*).

14. As per claim 17, Heirich discloses wherein transforming comprises performing an operation in the set: stretching, texture mapping, lighting, highlighting, translating from a first display format into a second display format, and applying a multi-dimensional transformation (c. 10 ll. 48-55: *The functions of core 110 include at least two computations: a Z comparison operation, in which one of the two input pixels is discarded based on their relative Z values, and a blend operation, in which transparent pixels are blended using a variety of blending formulas. Other pixel operations can easily be added to support commercially important markets, including image compositing and digital special effects*).

15. As per claim 18, Heirich discloses wherein the graphics arbiter receives per-pixel alpha information from the first display source and wherein the graphics arbiter uses the per-pixel alpha information received from the first display source to merge the display information from the first display memory surface set and from the second display memory surface set for transfer to the presentation surface set (c. 10 ll. 48-55: *The functions of core 110 include at least two computations: a Z comparison operation, in which one of the two input pixels is discarded based on their relative Z values, and a blend operation, in which transparent pixels are blended using a*

variety of blending formulas. Other pixel operations can easily be added to support commercially important markets, including image compositing and digital special effects).

16. As per claim 19, Heirich discloses a third display source distinct from the graphics arbiter, wherein the graphics arbiter reads a drawing instruction from the third display source and performs the drawing instruction to write to the presentation surface set (c. 10 ll. 32-37 and c. 11 ll. 1-2 and ll. 39-43: *under some circumstances, core 110 may take additional data from host buffer 140... the result data might be combined with additional data from host buffer 140... the data for each pixel might also include data on the nature of the computation to perform on that pixel, as well as the data to be used in that computation*).

17. As per claim 20, Heirich discloses wherein the drawing instruction instructs the graphics arbiter to perform an operation in the set: deinterlacing video, interpolating video (c. 11 ll. 35-39: *other operations could be defined in order to support digital effects and image processing. Some examples include pixel difference, min, max, dissolve, color filters, and the like*).

18. Claims 21-26, 28, 29, 34, 35, 37-42 are similar in scope to claims 1-4, 6-8, 13, 14, and 16-20, and are rejected under the same rationale.

Allowable Subject Matter

19. Claims 5, 9-12, 15, 27, 30-33, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art does not disclose or render obvious the combination of elements recited in the claims. Specifically, the cited prior art fails to disclose or render obvious the following

limitations: inhibiting a flip in the presentation flipping chain if the contents of the presentation back buffer with contents of a buffer immediately preceding the presentation back buffer in the presentation flipping chain match as per claims 5 and 27; graphics arbiter notifies the first display source of a first estimated time when a future frame will be displayed on the display device as per claims 9-12 and 30-33; the graphics arbiter provides occlusion information to the first display source as per claims 15 and 36.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication No. US 20040130558A1

U.S. Patent Nos. US006664968B2 US006473086B1 US006359631B2 US005850232A

B. Wei, D. Clark, E. Felten, and K. Li. Performance Issues of a Distributed Frame Buffer on a Multicomputer. In *Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics Hardware,* pages 87-96, August 1998.

S. Nishimura and T. Kunii. VC-1: A Scalable Graphics Computer with Virtual Local Frame Buffers. In *Proceedings of the 23rd Annual Conference on Computer Graphics and Interactive Techniques,* pages 365-373, August 1996.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
September 24, 2004